MOTOROLA

MC142100
MC145100

4 X 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

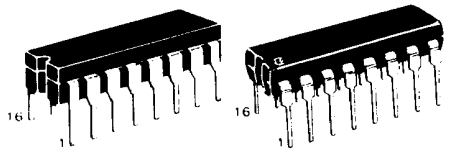
The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which controls the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In the MC145100, an internal power-on reset turns off all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset (MC145100 Only)
- Low On Resistance — Typically on 110 Ω @ 10 Vdc
- Large Analog Range (V_{DD}-V_{SS})
- All Pins Are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4 X 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

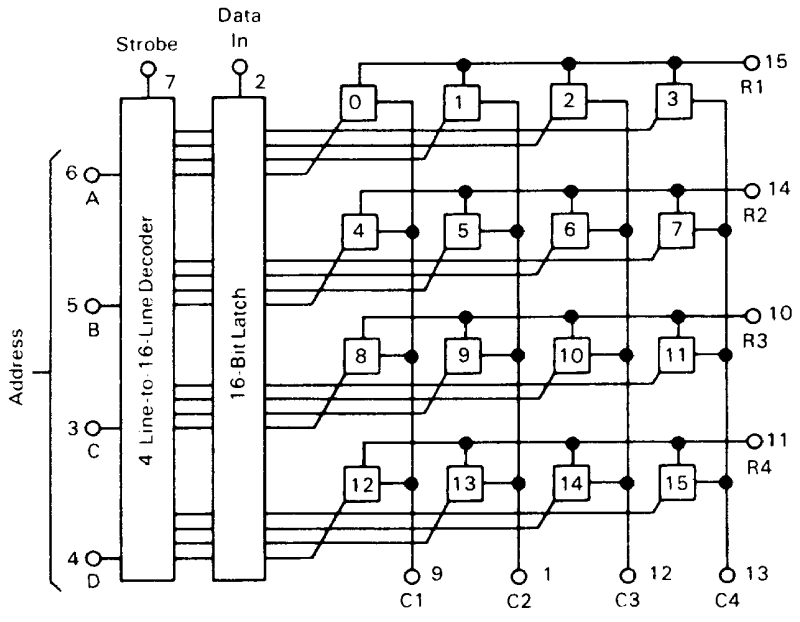


L SUFFIX
CERAMIC PACKAGE
CASE 620

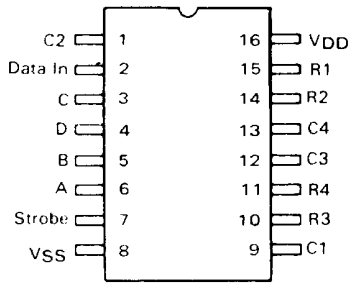
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



PIN ASSIGNMENTS



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused control inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).