MITSUBISHI BIPOLAR DIGITAL ICs

M54730AP, S/P, S-1/P, S-2
M54731AP, S/P, S-1/P, S-2

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

The electrical characteristics and programming conditions of the M54730P,S were changed to make the M54730AP,S.

DESCRIPTION

The M54730AP, S (open collector output) as well as the M54730AP,S (three state output) are field programmable ROM's with fuse links type 256 bit (32 word × 8 bit) memories.

FEATURES

- Access time:
  M54730AP, S-1/M54731AP, S-1 ..... 30ns (Max)
  M54730AP, S-2/M54731AP, S-2 ..... 35ns (Max)
  M54730AP, S/M54731AP, S ..... 50ns (Max)
- Unique built-in test circuits guarantee high programming yield as well as various performance characteristics after programming
- Fuse technology is used
- Memory capacity: 256 bits (32 words × 8 bits)
- Output type: M54730AP,S (open collector output)
  M54731AP,S (three state output)
- Output level befor programming is high
- Chip enable pin $\overline{E}$ provided for easy expansion of memory capacity
- Input and output are TTL compatible
- Package is 16-pin DIL ceramic or plastic

APPLICATION

General purpose, for use in industrial and consumer equipment

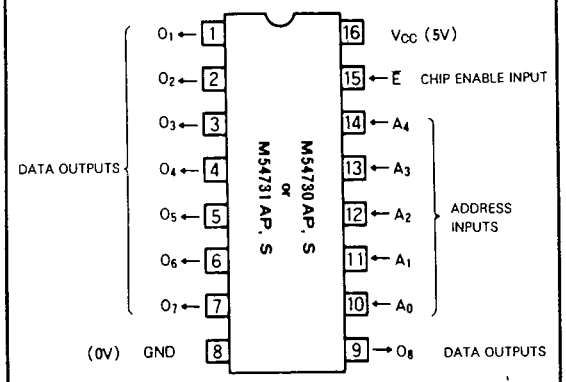
SUMMARY OF OPERATION

The unit consists of an address circuit, decoder circuit, memory circuit, output circuit, and a chip enable circuit. The memory cells are structured from fuses and diodes. Data can be programmed into the PROM by the user using a writer by cutting the fuses of the memory cells. Before programming, the output level is high. After programming, the output level becomes low.

The 256 bit memory is made up of 32 words with 8 bits associated with each word. Through the address inputs $A_0 \sim A_4$, one word out of the 32 is chosen and an 8-bit parallel output, $O_1 \sim O_8$, is obtained.

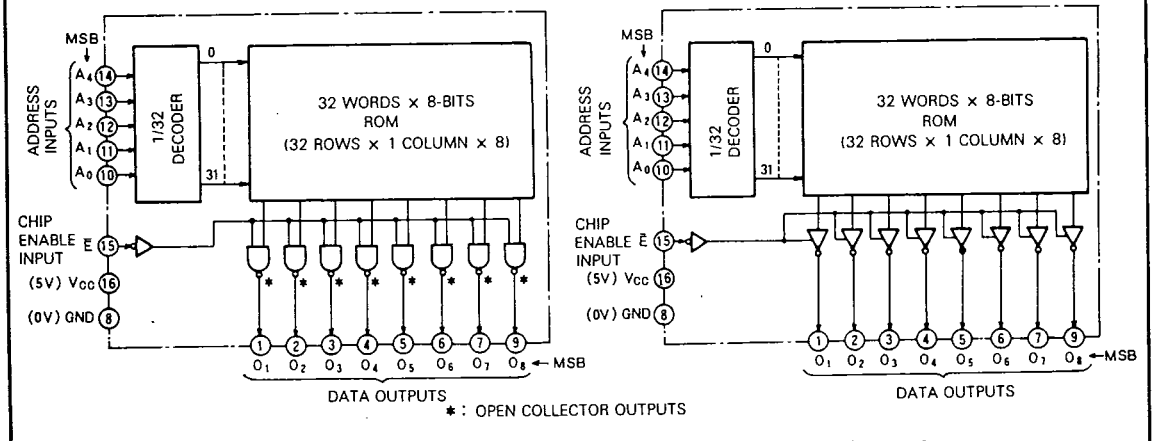
Input and output voltages threshold are the same as that for a TTL system and thus direct coupling can be made with TTL logic. Output is open collector (M54730AP,S) or 3-state (M54731AP,S) so AND ties are possible.

PIN CONFIGURATION (TOP VIEW)



Outline 16 S1 (M54730AS, M54731AS)
16 P4 (M54730AP, M54731AP)

BLOCK DIAGRAM



M54730AP, S M54731AP, S

MITSUBISHI ELECTRIC

M54730AP, S/P, S-1/P, S-2/M54731AP, S/P, S-1/P, S-2

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When the chip enable input $\overline{E}$ is at low level, the output is enabled and the content of the memory selected by the address input appears as output. When $\overline{E}$ is at high level, the output is disabled and regardless of the address input the output is high level (open collector output) or high impedance (3-state output).

READ-OUT FUNCTION TABLE (Note 1)

M54730AP,S Read-out function Table

$\overline{E}$	$O_1 \sim O_4$
L	Wn
H	H

M54731AP,S Read-out funciton Table

$\overline{E}$	$O_1 \sim O_4$
L	Wn
H	Z

Note 1: Wn: The memory content programmed in Wn word appears as output.
Z: High impendance state

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	When output is high level	−0.5 ~ +5.5	V
V_{OP}	Applied output voltage	During programming	21	V
$t_{W(P)}$ $t_{C(P)}$	Duty cycle	During programming	25	%
Topr	Operating ambient temperature		−20 ~ +75	°C
Tstg	Storage temperature		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High level output current (M54731AP/S) $V_{OH} \geqq 2.4V$	0		−2	mA
I_{OH}	High level output current (M54730AP/S) V_O=5V	0		50	μA
I_{OL}	Low level output current $V_{OL} \leqq 0.45V$	0		16	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.2	V
V_{OH}	High level output voltage (M54731AP, S)	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−2mA	2.4	3.1		V
I_{OH}	High level output current (M54730AP, S)	V_{CC}=5.25V, V_I=2V, V_I=0.8V, V_O=5V			50	μA
V_{OL}	Low level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OL}=16mA		0.3	0.45	V
I_{OZH}	Off-state High level output current (M54731AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=2.4V			50	μA
I_{OZL}	Off-state Low level output current (M54731AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High level input current	V_{CC}=5.25V, V_I=2.4V			40	μA
I_{IL}	Low level input current	V_{CC}=5.25V, V_I=0.4V		−100	−250	μA
I_{OS}	Output short-circuit current (M54731AP, S)(Note 2)	V_{CC}=5.25V, V_O=0V	−15		−100	mA
I_{CC}	Supply current (Note 3)	V_{CC}=5.25V, V_I=0V		70	100	mA
C_{IN}	Input capacitance	V_{CC}=5V, V_I=2V, f=1MHz		4		pF
C_{OUT}	Output capacitance	V_{CC}=5V, V_O=2V, f=1MHz		7		pF

* Typical values are at V_{CC} = 5V, T_a = 25°C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
3: I_{CC} is measured with all inputs at GND.

M54730AP, S/P, S-1/P, S-2/M54731AP, S/P, S-1/P, S-2

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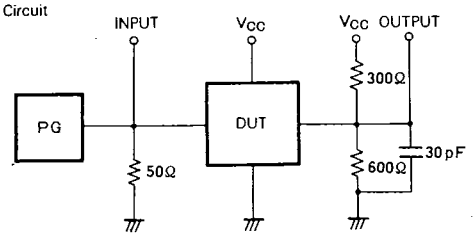
SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, T_a = 0 ~ 75°C, unless otherwise noted) (Note 4)

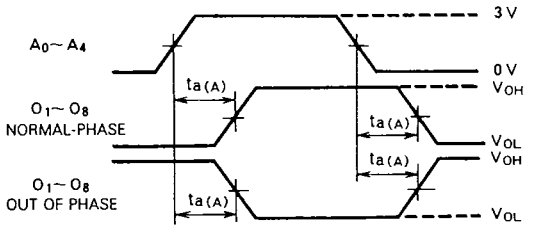
Symbol	Parameter	M54730AP, S-1 M54731AP, S-1			M54730AP, S-2 M54731AP, S-2			M54730AP, S M54731AP, S			Unit
		Limits			Limits			Limits			
		Min	Type	Max	Min	Typ	Max	Min	Typ	Max	
$t_{a(A)}$	Address access time		20	30		20	35		20	50	ns
$t_{a(\overline{E})}$	Chip enable access time		15	25		15	25		15	25	ns
$t_{CD(\overline{E})}$	Chip disable time		15	25		15	25		15	25	ns

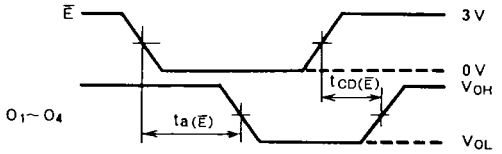
Note 4: Test Circuit



1. PG characteristics: t_r = 6ns, t_f = 6ns, PRR = 1MHz, t_{PW} = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
2. The electrostatic capacitance of the load includes probe and jig capacitance.

TIMING DIAGRAM (Reference Voltage = 1.5V)





RECOMMENDED OPERATING CONDITIONS FOR PROGRAMMING (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{IH(P)}$	High level input voltage	2.4	5	5	V
$V_{IL(P)}$	Low level input voltage	0	0	0.4	V
$V_{O(P)}$	Applied output voltage	20	21	21	V
$t_{W(P)}$	Applied pulse width	0.05	0.18	50	ms
$t_{W(P)}$ $t_{C(P)}$	Duty cycle		20	25	%
t_r	Pulse rise time	5	10	30	μs
$N_{(P)}$	Number of pulse applied	1	4	4	—
$V_{CC(P)}$	Supply voltage during programming	4.9	5	5.1	V
I_{OP}	Output applied current			100	mA
$V_{CCL(V)}$	Low level supply voltage for check after programming	4.4	4.4	4.5	V

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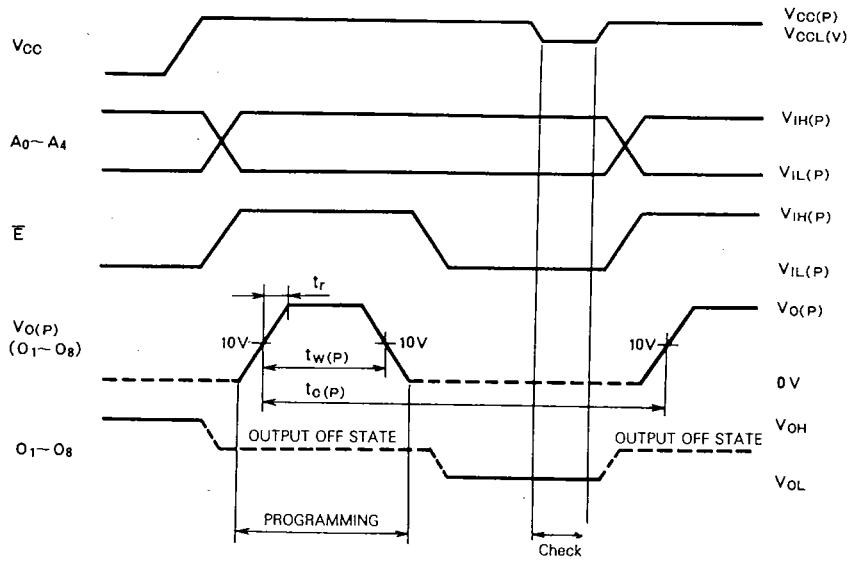
PROGRAMMING TIMING DIAGRAM



Note 5: $V_{O(P)}$ is the wave form applied to the output during programming. O_1-O_8 are the waveforms showing the output of the element itself.

PROGRAMMING METHOD

The elements actually programmed are the fuses making up the 256 memory cells. When the memory cell is not programmed, the output is logic high level (fuse closed). To put these at logic low level, the following steps are taken.

(1) Apply $V_{CC(P)}$ supply voltage (5V Typ)
(2) Select the word to be programmed by using the address inputs $A_0 \sim A_4$ (Input voltage: $V_{IH(P)}$ 5V Typ, $V_{IL(P)}$ 0V Typ)
(3) Put the chip enable input, $\overline{E}$, at high level ($V_{IH(P)}$ 5V Typ) and put the output in the OFF state.
(4) An output pulse $V_{O(P)}$ (21V Typ) is applied to the output corresponding to the bit to be programmed. $V_{O(P)}$ must be applied to each individual output; do not apply it to two or more outputs at the same time.
(5) Put $\overline{E}$ at low level ($V_{IL(P)}$ 0V Typ)
(6) Put the supply voltage at $V_{CCL(V)}$ (4.4V Typ) and check whether programming was completed or not.
(7) If the test in step (6) is passed, repeat steps (1) through (6) for the next bit or word to be programmed. If the test in step (6) is not passed, repeat steps (1) through (6). If these steps are repeated four times and test results are not positive, the IC can be considered defective.

For timing, refer to the programming timing diagrams.